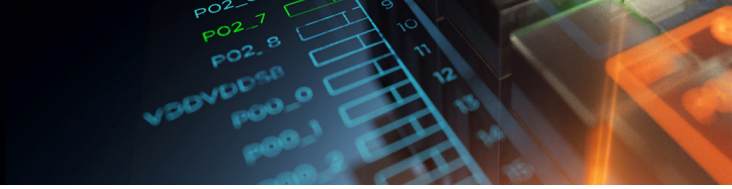
TASKING®

PIN MAPPER for AURIX™

Product Overview

PIN MAPPER FOR AURIX™



HIGH-LEVEL OVERVIEW

The TASKING Pin Mapper for AURIX tool helps you configure the device using the settings to automatically generate initialization code for the AURIX. The TASKING Pin Mapper can save a substantial amount of time for developers and provides assurance than no pin conflicts exist. In addition, the pin mapper generates a data file for PCB design, eliminating the chance for errors when passing data manually.

At the start of a project the system requirements have to be mapped to the device architecture, and the proper interconnections between peripheral modules (connectivity mapping) and interconnections from peripheral modules to physical pins (pin mapping) have to be activated.

Advanced microcontrollers such as AURIX are equipped with a large number of peripheral modules, but the limited number of pins on the chip do not allow all modules to be used simultaneously. The TASKING Pin Mapper functionality eases the developer's complex challenge of configuring hardware registers that are used for routing signals between peripherals, and assigning peripheral module I/Os to physical pins. This is accomplished using an interactive visual representation of peripheral modules and pins that the user can configure and review interconnections and properties. This saves you from the tedious task of maintaining an overview of the pin assignments in spreadsheets.

The pin mapper tool validates the configuration settings and immediately warns the user if conflicts arise. Such conflicts can be solved by hand by making other connections, but when most device pins are already in use, it can be quite cumbersome and complex to solve conflicts. The built-in Pin Conflicts Solver automates this task and will solve most conflicts for you. The TASKING Pin Mapper tool detects and resolves issues during software construction, whereas traditionally configuration errors remain hidden until the software is tested. The pin mapper reduces developer hours spent as well as the cost of test infrastructure.

The pin assignments as used by the software must match with the pin assignments of the printed circuit board design. To reduce the chance of miscommunications between software and hardware development teams the TASKING Pin Mapper also generates a pin configuration file that serves as input for PCB design software tools which translate the data (chip identifier, pin assignments and signal names) into a schematic symbol block.

FUNCTION AND FUTURE

Use Cases

The tool serves a number of different use cases such as:

- **Feasibility studies**

  You can quickly analyze whether it is possible to configure a particular device to satisfy a specific set of peripheral and I/O requirements.
- **Optimize hardware device costs**

  Search for the lowest cost device that supports the peripheral and I/O features listed in the system requirements. Features such as changing the device while the configuration is maintained and the ability to import the configuration from an existing project ease such tasks.
- **Create device initialization code**

  Once a configuration has been created and validated the corresponding device initialization code is generated in ISO-C format.
- **Re-use**

  Studies reveal that 60 to 80 percent of requirements, code and tests are shared among projects. The pin mapper enables you to re-use and modify device configurations from earlier projects.

- **Improve information exchange between software and hardware development teams**

  Generate a pin configuration file that serves as input for PCB design software tools which contains chip identifier, pin assignments and signal names.

- **Analyze whether a device configuration can be adapted for a given PCB layout**

  If you have a fixed hardware design and must switch to a different type of microcontroller the tool assists you to explore the proper software configuration.

User Interface

Interaction with the TASKING Pin Mapper is established via the Eclipse TASKING Pin Mapper Perspective. Once a device is selected the following views are shown.

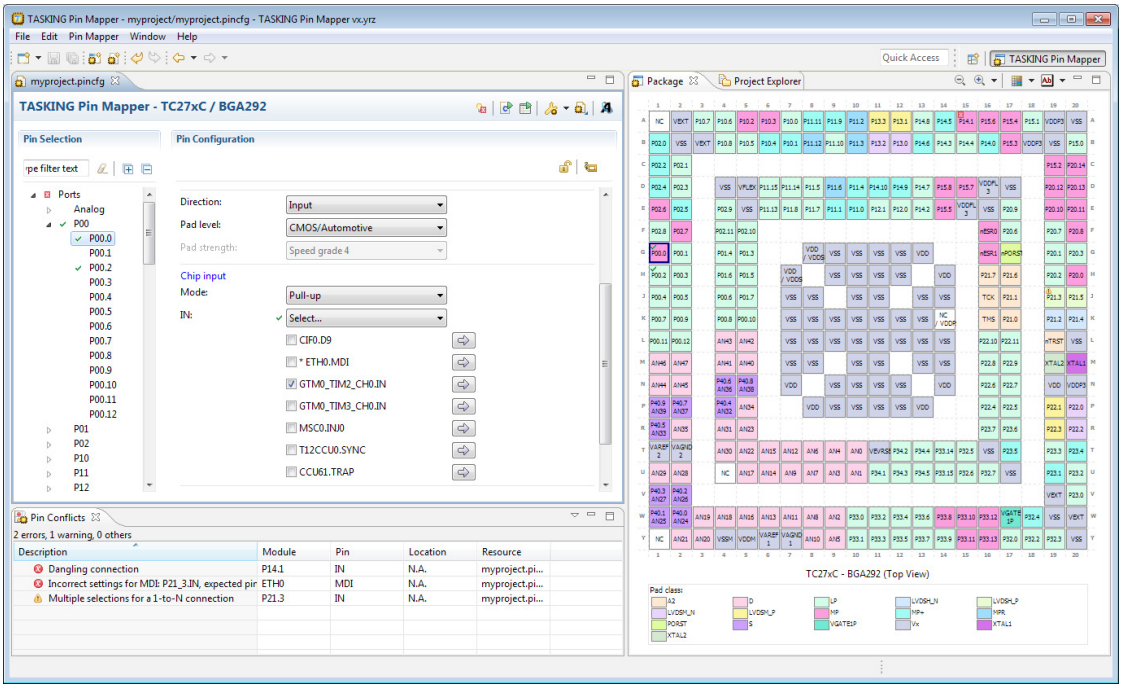


Figure 1: TASKING Pin Mapper GUI

- **Pin Selection Pane**

  Resource and connectivity mapping lets you identify the proper peripheral module for the required functionality and to define the necessary connections. The Pin Selection pane provides access to all peripheral modules, I/O ports, and other pins (e.g. VDD) and lets you select a specific component.

- **Pin Configuration Pane**

  The Pin Configuration pane shows the current configuration settings of the selected component and enables you to change the settings. Attributes such as a signal connections, the reset state, power domain, signal mode, et cetera can be specified.

- **Pin Conflicts View**

  Feedback about conflicts in your configuration is listed in the Pin Conflicts view, and is provided immediately when a conflict occurs. TASKING Pin Mapper provides an automated conflict resolution mechanism. You can also lock a configuration item to ensure that it will not be considered by this resolution mechanism.

- **Package View**

  The Package view shows the device pins, in this case for a BGA package and provides information about the pin's status.

Solving Configuration Conflicts

Configuration issues can be resolved by hand or automatically by the tool. Figure 2 shows a list of conflicts and the actions that will be taken by the tool to resolve the conflicts. If desired, you can override a suggested action, or lock a connection in order to hide it from the solver.

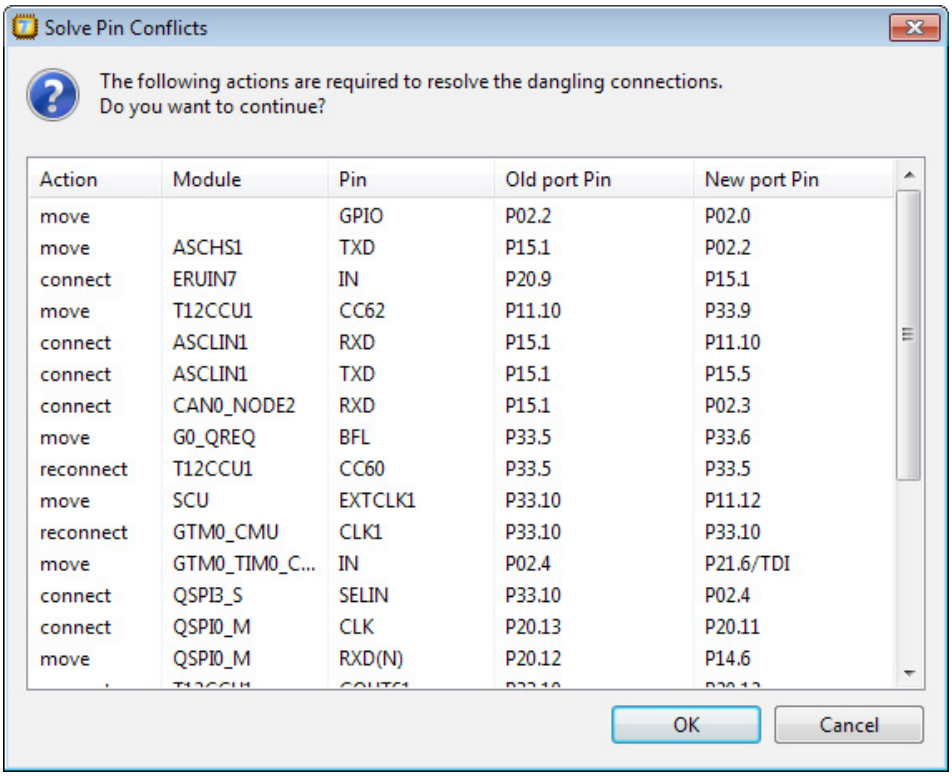


Figure 2: Resolving Configuration Conflicts

Depending on the projected calculation time, the solver either performs an exhaustive search or applies a heuristic partial search algorithm to find a solution. In case of a partial search it is possible that a solution does exist while the solver does not find it, the user is notified about such cases.

Code Generation

Once the device is configured and there are no conflicts, the tool emits initialization code for all GPIOs as well as port pins connected to peripheral modules. The code is in ISO-C format and can be compiled with compilers from TASKING or other suppliers.

The configuration can also be saved in comma-separated values (CSV) format for import in a spreadsheet.

A pin configuration file can also be exported to a PCB design software tool.

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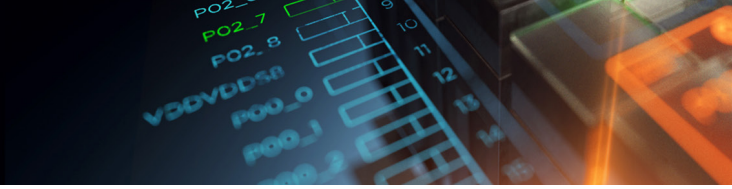

PRODUCT SPECIFICATIONS

Availability and compatibility:

- TASKING Pin Mapper for AURIX is distributed as an integral part of the TASKING VX-toolset for TriCore; it is included in all editions of the toolset.
- TASKING Pin Mapper for AURIX is also available as stand-alone product and is compatible with any ISO-C compliant compiler for AURIX.

Supported host systems:

- 64-bit versions of Windows 7 or higher

Supported TriCore Devices:

- AURIX Family (TC22x, TC23x, TC26x, TC27x, TC29x).
- AURIX 2G Family (TC38x, TC39x).

Eclipse Version:

- Mars

Compatible PCB design software:

- Altium Designer

SUMMARY

The TASKING Pin Mapper for AURIX has been jointly developed with Infineon and contains expert-level knowledge about the dependencies between between peripheral modules and device pins. The tool enables both novice and expert users to quickly configure AURIX microcontrollers. It provides the vital functionality to executed feasibility studies, select the lowest cost hardware device for a given set of requirements, and to create device initialization code in the most cost-effective way.

ABOUT ALTIUM

Altium LLC (ASX: ALU) is a multinational software corporation headquartered in San Diego, California, that focuses on electronics design systems for 3D PCB design and embedded system development. Altium products are found everywhere from world leading electronic design teams to the grassroots electronic design community.

With a unique range of technologies Altium helps organisations and design communities to innovate, collaborate and create connected products while remaining on-time and on-budget. Products provided are Altium Designer®, Altium Vault®, CircuitStudio®, PCBWorks®, CircuitMaker®, Octopart®, Ciiva® and the TASKING® range of embedded software compilers.

Founded in 1985, Altium has offices worldwide, with US locations in San Diego, Boston and New York City, European locations in Karlsruhe, Amersfoort, Kiev and Zug and Asia-Pacific locations in Shanghai, Tokyo and Sydney. For more information, visit www.altium.com. You can also follow and engage with Altium via Facebook, Twitter and YouTube.