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TAKE ADVANTAGE OF INFINEON AURIX TC3XX FAMILY WITH THE RIGHT COMPILER

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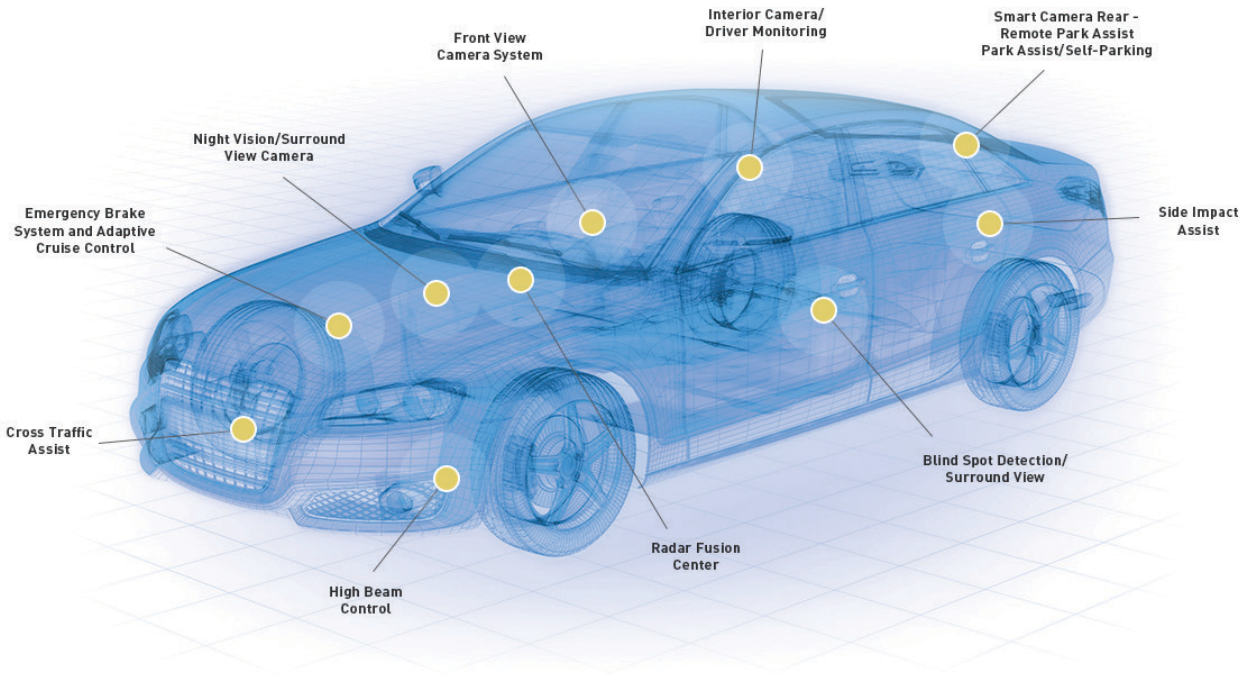
INTRODUCTION:

There's no question that the automotive industry is becoming more dependent on electronics. Advanced driver assistance systems (ADAS), radar, sensor fusion, and in-vehicle infotainment (IVI) systems all provide a wide range of capabilities, such as telematics, safety systems, entertainment, communication, and information connectivity. It's estimated that electronics account for at least 30 percent of an automobile's total production cost.(1) New cars may contain 20 to 70 electronic control units, with more than 100 million object code instructions (about 1 GB of software).(2)

It is increasingly important that control units offer features that address the industry's high-reliability and quality requirements, as well as ever-increasing performance demands. But it is just as necessary for embedded software compilers and linkers to be able to take advantage of these features through programming and performance optimizations.



INTRODUCING THE INFINEON AURIX TC3XX FAMILY TRICORE PROCESSOR

Real-time performance and embedded safety and security features make the TriCore™ family a perfect match for the transportation industry. With its special feature set and its safe as well as high-performance TriCore cores, AURIX TC2xx Family is the ideal platform for a wide range of automotive applications including the control of combustion engines, electrical and hybrid vehicles, transmission control units, chassis and powertrain applications, braking systems, electric power steering systems, airbags, radar, sensor fusion, IVI systems, and ADAS.

The AURIX TC2xx Family architecture consists of up to six independent, high-performance 32-bit superscalar TriCore V1.6.2 CPUs running at up to 300 MHz over the full automotive temperature range. The architecture has been developed according to an audited ISO26262-compliant process and designed to meet ASIL-D on an application level. AURIX TC3xx Family processor includes a number of features that allow automotive software architects to maximize the performance of their applications:

- Multicore lockstep architecture
- Flexible memory management using near and far memory with Error-Correcting Code (ECC)
- Integrated hardware security module (HSM)
- Superscalar cores (TriCore)
- Integrated generic timer module (GTM)
- Support for hardware Fast Fourier Transform (FFT)

Software architects can benefit substantially from each of these features, many of which work best if both the compiler and linker support direct access to them.

THE POWER OF MULTICORE ARCHITECTURE

Many embedded automotive applications are subject to stringent safety requirements. One way to meet these requirements is to use the lockstep technique, in which the main core and the lockstep core run the same software in parallel to detect execution errors. Legacy systems require two processors to run lockstep code. But with the AURIX TC3xx Family TriCore processor, lockstep can be achieved with a single processor, because four of the six cores feature additional lockstep cores (Figure 2), enabling a new level of ISO26262 functional safe computational power on a single integrated device — reducing development effort and cost while still achieving ASIL-D compliance.

LOCKSTEP EXPLAINED

When two processors (or cores) are initialized to the same state during system start-up and they receive the same inputs (code, bus operations, and asynchronous events), they are said to be operating in lockstep. That is, during normal operation the state of the two processors or cores is identical from clock to clock. The lockstep technique assumes that an error in either processor will cause a difference between the states of the two processors, which will eventually be manifested as a difference in the outputs. If that occurs, the discrepancy is flagged as an error and the appropriate corrective action can be taken.

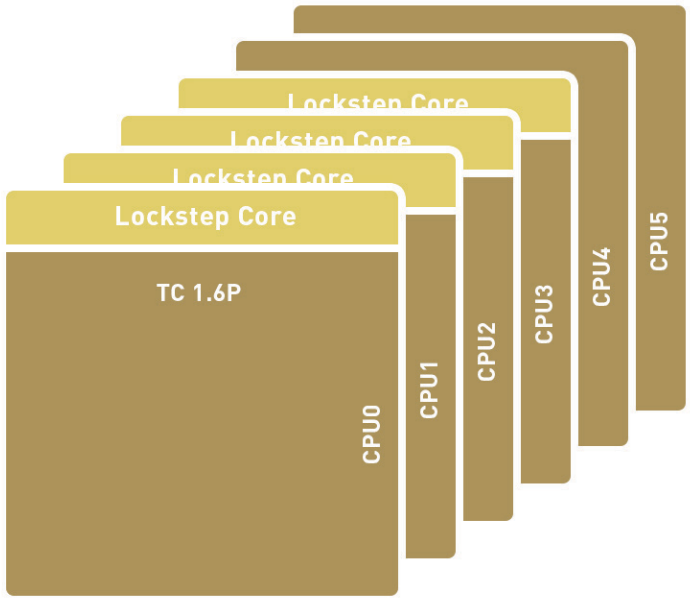


Figure 1. The AURIX TC3xx Family TriCore processor's multicore architecture enables safe computational power on a single integrated device.

AURIX TC2xx Family lockstep architecture is designed to control and mitigate failures caused by physical isolation, instruction-level execution diversity, and circuit-level design and timing diversity. Special features include a two-cycle delay, special design of clock and reset networks, and an innovative design of the lockstep comparator.

The AURIX TC2xx Family diverse lockstep cores have been additionally transformed to provide architectural hardware diversity and further reduce common-cause failures (Figure 2).

Multicore architecture is a powerful tool and can substantially increase application safety. However, it is the software architect's responsibility to ensure that the software is making most efficient use of the cores through the use of an optimized compiler and linker.

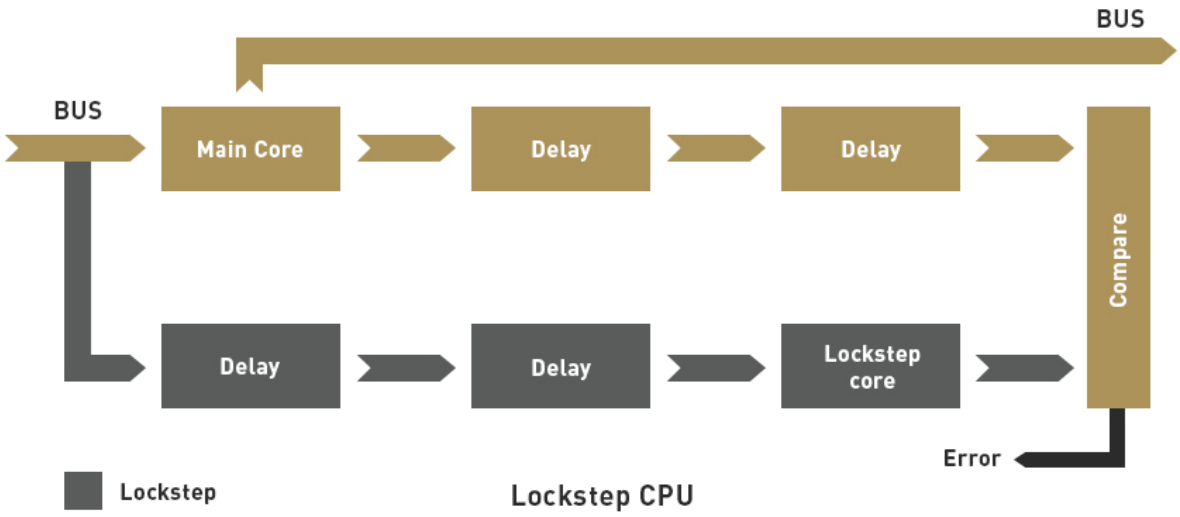


Figure 2. Architectural hardware diversity between the main core and the lockstep cores helps reduce common-cause failures. Courtesy Infineon.

MAKING THE MOST OF MEMORY

The explosive growth of electronic systems in modern cars has significantly impacted the market demand for semiconductor memory. However, not all memory is created equal. The AURIX TC3xx Family TriCore processor's memory architecture offers several types of memory, including ECC protection, for the most flexibility in application design:

- **Scratchpad memory.** Each core provides a limited amount of data scratchpad RAM (DSPR) and program scratchpad RAM (PSPR). Also known as near memory, this type of memory can be addressed on each core without using the bus, and therefore access is extremely fast. To maximize application performance, developers can map performance-critical code segments to use near memory. Although it is possible to access DSPR and PSPR on other cores, this does require the bus and takes longer—it is generally done only for one-time configuration at start-up.
- **Flash memory.** Each core also offers Flash memory, which is read-only and persistent. Flash memory capacity is significantly larger than scratchpad memory, but is slower to access.
- **RAM.** This type of memory is not persistent, but supports both read and write access. Like Flash, RAM capacity is significantly larger than scratchpad memory but is slower to access.

To take best advantage of the TriCore processor's flexible memory architecture, the designer must be using a compiler that is aware of the various types of memory that are available, and the linker must allow memory mapping configuration (Figure 3).

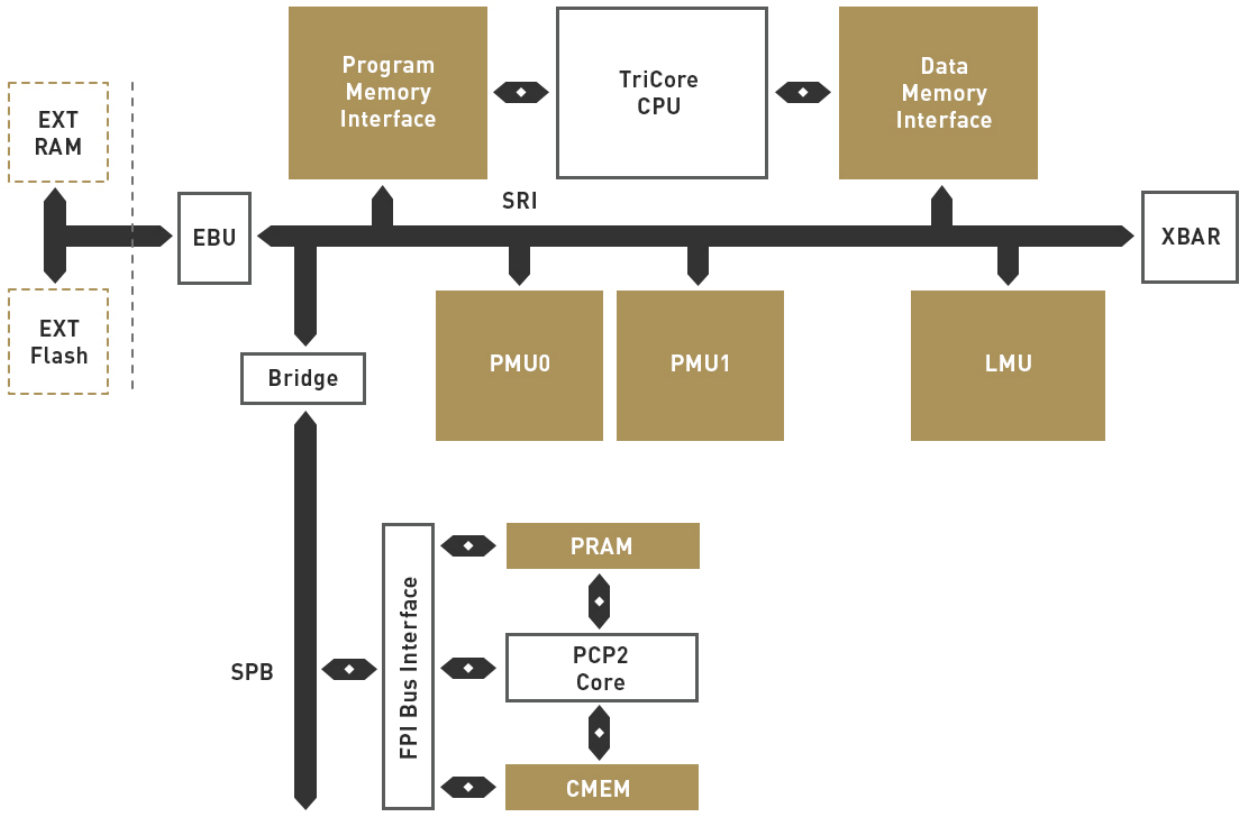


Figure 3. A flexible memory architecture helps software architects meet the growing market demands for memory performance.

SUPERSCALAR CORES

The AURIX TC3xx Family TriCore processor is superscalar – that is, each core implements instruction-level parallelism, resulting in the ability to execute more instructions than would otherwise be possible at a given clock rate. (3)

Each core features a pipeline that issues to several execution units, each of which can execute one instruction per cycle (within certain constraints). One unit primarily handles data arithmetic instructions and data-conditional jumps; another mainly handles load/store memory accesses, address arithmetic, unconditional jumps, calls, and context-switching operations. The third unit is used mainly for loop instructions. As instructions are executed in parallel, the processor performs automatic data resource hazard checking and handling.

In addition to writing performance-conscious applications that take advantage of superscalar cores, software architects can significantly improve their application's performance by compiling their code with a compiler that is optimized for the TriCore pipeline.

PROTECTING APPLICATIONS WITH THE INTEGRATED HARDWARE SECURITY MODULE

Some automotive applications are subject to specific security functionalities, such as tuning protection, immobilizer systems, and secure onboard communication. These types of applications must be protected against vehicle intrusion threats including IP infringement, fraud, and software hijacking.

The AURIX TC3xx Family TriCore processor features an integrated HSM that provides a secure computing platform consisting of a 32-bit CPU, special access-protected memory for storing the cryptographic key and the unique subscriber identifiers, a hardware accelerator for the state-of-the-art AES-128 encryption, and specific hardware for random number generation (SHE, PRNG, and TRNG). A firewall separates the HSM from the rest of the AURIX TC2xx Family processor (Figure 4), enabling the HSM to function as an anchor of trust. The HSM was developed in line with the EVITA (E-safety Vehicle Intrusion proTected Applications) project.

The HSM is a highly flexible and programmable solution. It includes key management for up to 20 keys, and whereas AES-128 and TRNG are implemented in the hardware, customer-specific requirements, such as HASH algorithms or asymmetric encryption, can be programmed via software. Secure key storage is provided by a separated HSM-DFLASH section, but alternative secure key storage is feasible using dedicated HSM-PFLASH sections. The SHE+ software driver controls the hardware security peripheral in the HSM domain and interacts with the TriCore host core. SHE+ comes with the AUTOSAR CRY interface for integrating the HSM security features into an automotive application, including an interface to AUTOSAR, communication from the host core to the HSM and vice versa, key storage functionality, and security peripheral drivers.

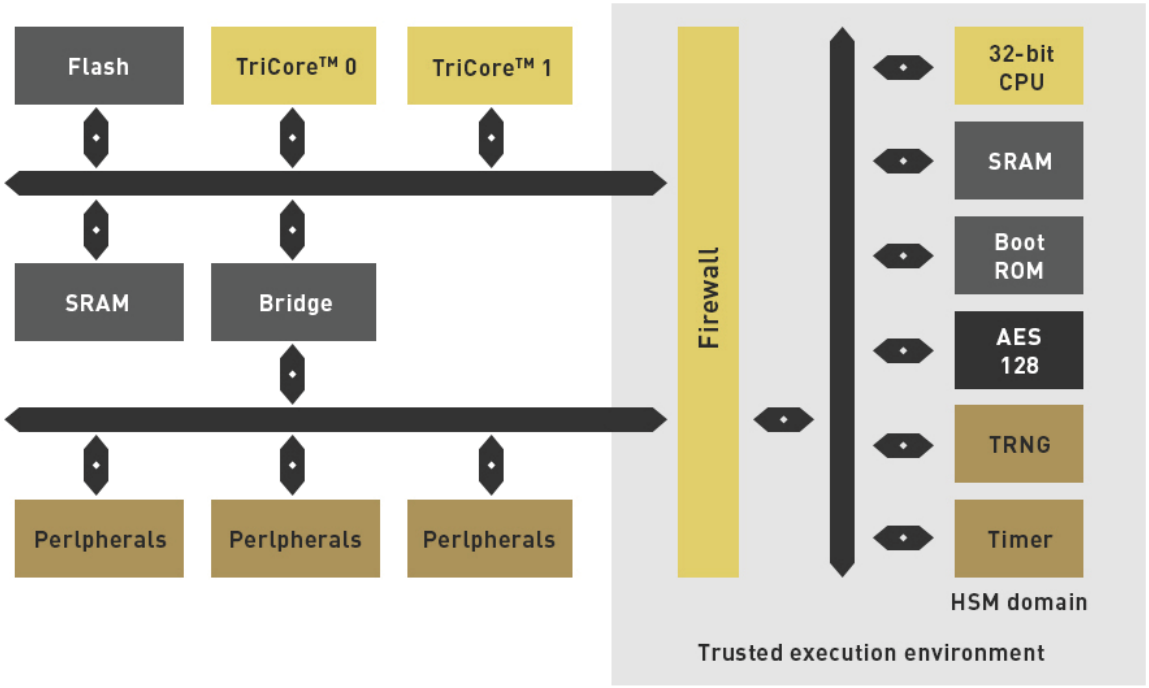


Figure 4. The AURIX TC3xx Family TriCore processor's integrated hardware security module (HSM) acts as an anchor of trust for security-sensitive automotive applications like immobilizers and secure onboard communications. Courtesy of Infineon.

Most security modules are programmable only in assembly language; some compilers support programming the AURIX TC2xx Family TriCore HSM in C, making code development simpler and faster.

SUPPORT HIGHLY COMPLEX, TIME-CRITICAL APPLICATIONS WITH THE INTEGRATED GENERIC TIMER MODULE

Timer modules are employed in Electronic Control Units (ECUs) to perform real-time signal processing in the millisecond or sub-millisecond range. Historically, timer modules have been either hardware-centric or software-centric. Both approaches have drawbacks: hardware-centric timer modules are dependent on the host CPU, leading to platform dependencies that hinder standardization. Software-centric timer modules have higher latency. (3)

The AURIX TC3xx Family TriCore processor uses a new approach, called a generic timer module (GTM). The primary task of the GTM is to offload work from the CPU by handling fast repetitive tasks and minimizing the number of interrupts needed to be raised. This is achieved with a number of programmable hardware modules that, after initialization, can work independently, without the need to constantly interrupt the CPU.

The GTM combines both hardware-centric and software-centric approaches using a unique architecture that supports both pre-implemented hardware functions as well as a multichannel sequencer (MCS), which is a simple programmable processing core. In this way, the GTM can execute complex functions in software while guaranteeing low latency and full timing predictability.

The GTM's modular design makes it easy to add and remove features in a system without affecting the existing ones—simplifying development and moving toward platform independence. Like the HSM, the GTM can be programmed using C as well as assembly, providing the chosen compiler supports C.

In one study of an early version of an AURIX TC2xx Family GTM, researchers found that the GTM can, thanks to its design with independent hardware modules, sustain a higher throughput and a more deterministic latency than legacy timer modules. (4)

SUPPORT FOR HARDWARE FFT

ADAS applications often use radar systems, which in turn rely greatly on the FFT capabilities of the microprocessor, which transform the radar frequencies into spatial information. By nature, FFT functions are computationally intensive; the TriCore processor provides highly efficient, hardware FFT processing that can enhance the performance of radar systems, thereby enabling energy-efficient solutions. (5) (6)

Radar processing is often prototyped on high-end processors that, unlike embedded devices, have a lot of extra horsepower to do the FFT in software. Now, ADAS developers can easily port their applications from high-end cores to an embedded device, using the TriCore processor's dedicated hardware FFT acceleration unit.

The TriCore processor provides the necessary hardware and software support to enable the user building embedded ADAS applications up to ASIL-D, meaning that they can be involved in automatic decisions to assist drivers, such as emergency braking.

TIGHTLY COUPLED COMPILER AND HARDWARE PRODUCE THE BEST RESULTS

As the automotive industry relies more and more on electronics to power ADAS, radar, sensor fusion, and intelligent IVI systems, the AURIX TC3xx Family TriCore processor is a logical choice for applications that must meet stringent high-performance, safety, and data security requirements. Important features include multicore lockstep capabilities, flexible memory architecture, and superscalar cores, combined with integrated hardware security and GTMs and support for hardware FFT. To take full advantage of these features, software architects must produce code that accesses them and choose a compiler and linker that are tightly coupled to the hardware.

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Product Brief

AURIX TC3xx Family Brief

AURIX TC2xx Family Details

Hardware Security Module

Generic Timer Module

Application Performance Optimization