TASKING.

Programming the Bosch[®] GTM Using the Traditional C Array Approach

int n; // left, shared with SoC cor / below, future release in

#if ((10'_VERSION_)+_REVISION_) <= 3001
inline int _get_sta(void) {return STA;}
inline void _set_sta(int x) {STA=x;}
#endif</pre>

void __channel(l) getversion(void)
{ /* relay MCS compiler version to SoC *
 n = __VERSION_;
 __set_sta(__get_sta()|2);

void _channel(2) getrevision(void)

/* relay MCS compiler revision to SoC 7/

n = __REVISION_;

set_sta(_get_sta()|2);

Int main(void)

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Henk-Piet Glas

Technical Product Specialist

PROGRAMMING THE BOSCH® GTM USING THE TRADITIONAL C ARRAY APPROACH

INTRODUCTION

Today's multi-core technology expects toolset vendors to extend their compiler toolset with add-on compilers for specialized 'guest' cores alongside the main CPU. An AURIX[™] core, for example, is equipped with multiple TriCore[®] cores, an HSM core, an SCR core and a GTM core, each requiring their own specific compiler while being tightly connected in terms of actual silicon. The **TASKING tool suite** provides fully integrated compilers allowing you to target code for the primary CPU and any of its guest cores.

Not every toolset vendor stays up to par with the latest developments and there has been an increasing demand to offer a commercially available standalone MCS C compiler that can be used in conjunction with third-party compilers. In such a symbiosis, the partnership supports both the primary CPU, using a third-party compiler, and the add-on MCS core using TASKING. This demand heralded the advent of the standalone **TASKING VX-toolset for MCS** - a compiler capable of building unexpected relationships. More accurately, this compiler allows for programming the MCS on **RH850**, Power Architecture and AURIX[™] architectures.

The standalone **TASKING VX-toolset for MCS** was developed in collaboration with Bosch[®]. A key feature to establish integration is the locator's ability to generate a C array output containing the MCS program image, a feature inherited from the original Bosch[®] assembler. Using a minimalistic sample case, this paper discusses its format and shows how to correlate it to your map file. Also we explain how to integrate the C array code into a project of any third-party compiler; running the sample code as a proof of concept.

But like with any good story you need to start at the beginning. We will be exploring what spawned all of this into existence and how it will impact the future.

THE GTM ARCHITECTURE

The Bosch® GTM core implements a generic timer platform for complex applications in the automotive industry like power train, power steering, chassis and transmission control. To serve these different application domains, the GTM provides a wide range of timer functions like counters, multi-action capture/compare, PWM functions, duty-cycle measurements and more.

In addition, the GTM includes internal RISC-like programmable cores for data processing and complex output sequence generation [1]. These cores are called multi-channel sequencer cores, or MCS cores for short. Its IP, now capable of being programmed through the TASKING standalone MCS C compiler, is designed to run with minimal CPU interaction while unloading the CPU from handling interrupt service requests as much as possible.

The GTM design is owned by Robert Bosch[®] GmbH. An SoC design can incorporate its IP alongside the main CPU using one or more GTM instances. Each GTM can have one or more MCS cores, and each MCS core implements 8 channels.



MCS AND CPU SAMPLE PROGRAMS

Listed below is the sample program that will be used throughout the course of this paper. The sample program consist of two parts. The first part shown below in *Figure 1* (left) is the code that will run on an MCS core. The second part in *Figure 1* (right) is the code that will run on the hosting architecture (SoC) and interact with the generic timer module (GTM). The sample code is minimalistic in nature, since the aim is not to go deep in terms of functionality, but instead demonstrate what you need to do to hook up your application code into the project of your compiler.



Figure 1 - Sample program for an MCS core

MCS PROJECT SETTINGS

The MCS core project settings primarily consist of default settings. Those noteworthy to building the application are:

- 1. Processor Settings
- 2. Linker Map File
- 3. Linker Output Format

Of each of these you'll find snapshots listed below. Note that the version of the MCS core is 3.0 and that the target code is configured for core mcs00. Further note that the project uses the classic map file generation listing only the locate result. Finally note that the linker output format has been set to C array.



EXTENDING YOUR THIRD-PARTY IDE WITH TASKING® VX-Toolset FOR MCS

perinter text	Processor
 Resource Builders C/C++ Build Build Variables Environment Logging Memory Processor Stack/Heap C/C++ General Project References Run/Debug Settings 	Configuration: Debug [Active] Processor selection
	Multi-core configuration

🔽 Generate map file (.map)	
📃 Generate XML map file forma	t (.mapxml) for map file viewer
Include call graph information	n
Include processed files inform	ation
Include information on invoc	ation and tools
Include link result information	1
🔽 Include locate result informat	ion
Include memory usage inform	nation
Include information on remov	ved sections
Include information of non-al	lloc sections
Include overlay information	
Include module local symbols	information
Include cross references information	mation
Include processor and memory	ry information
Include locate rules	

🔲 Generate	Intel Hex format file	
Cenerate	S-records file	
🔽 Generate	C array file	
Create file	e for each memory c	hip
Size of addre	sses (in bytes) for Int	tel Hex r
Size of addre	sses (in bytes) for M	otorola
🛛 Emit start	address record	
🔽 Emit list o	of exported symbols	

Figure 2 - MCS project settings - processor settings (top), linker map file (middle) linker output format (bottom)

CORRELATING AND LOCATING RESULTS OF A C ARRAY FOOTPRINT

Now that the MCS project has been set up, you can proceed to build. A few files will be generated as a result:

- cinfo_gtm30_05_mcs00.c(C file below)
- cinfo_gtm30_05_mcs00.h (H file below)
- cinfo.map (map file below)

The *C file* contains the MCS program image footprint poured into an array. This includes both code and data. The *H file* contains offsets within the array pointing to functions and global variables. This essentially creates a symbol table. Since the MCS core is memory mapped within the hosting architecture, the combination of these two files allows the third-party compiler to (a) locate the program image at its designated base address and (b) peek or poke MCS data or code. Listed below are snapshots of both the *C file* and *H file*.

cinfo_gtm30_05_mc	s00.c 🖾
⊕ * Generated	by TASKING VX-toolset for MCS:
#include "cin	fo_gtm30_05_mcs00.h"
unsigned long	cinfo_gtm30_05_mcs00[] = {
0xE0000078,	/* 0 */
0xE0000044,	/* 1 */
0xE0000024,	/* 2 */
0xE000000C,	/* 3 */
0xE0000010,	/* 4 */
0xE0000014,	/* 5 */
0xE0000018,	/* 6 */
0xE000001C,	/* 7 */
0x00000000,	/* 8 */
0x15000002,	/* 9 */
0xA5020020,	/* 10 */
0xA5800000,	/* 11 */
0x55000002,	/* 12 */
0xA8500000,	/* 13 */
0xA2800000,	/* 14 */
0x42FFFFFE,	/* 15 */
0xA8200000,	/* 16 */
0x15000BB9,	/* 17 */
0xA5020020,	/* 18 */
0xA5800000,	/* 19 */
0x55000002,	/* 20 */
0xA8500000,	/* 21 */
0xA2800000,	/* 22 */







The best exercise to get an understanding of the C array program image footprint is to try and correlate some of its *H file* symbols to actual addresses in the map file or the simulator's disassembly window. As an example let's try to cross-reference function getrevision in *Figure 4* below (note that the snapshot is folded to increase resolution).

extern unsigned long cinfo gtm3	0 05 mcs00[]:		
/* Locations of symbols as inde	x in the associ	iated C array	*/
#define CINFO_GTM30_05_MCS00_ge	tversion 17		
#define CINFO GTM30 05 MCS00 n	8		
<pre>#define CINF0_GTM30_05_MCS00_ge</pre>	trevision 9		
<pre>#define CINFO_GTM30_05_MCS00_ma</pre>	in 25		
<pre>#define CINFO_GTM30_05_MCS00</pre>	vector.1 17 '	*/	
/* #define CINFO_GTM30_05_MCS00	vector.2 9 */		<u> </u>
#define CINFO_GIM30_05_MCS00	START 30		
٠	1		
Section	Size (MAU)	Space addr	Chip addr
Section .vector.0 (48)	Size (MAU)	Space addr 0x0	Chip addr 0x0
Section .vector.0 (48) .vector.1 (47)	Size (MAU) 0x00000004 0x00000004	Space addr 0x0 0x00000004	Chip addr 0x0 0x00000094
Section .vector.0 (48) .vector.1 (47) .vector.2 (46)	Size (MAU) 0x00000004 0x00000004 0x00000004	Space addr 0x0 0x00000004 0x00000008	Chip addr 0x0 0x00000004 0x00000008
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x0 0x00000004 0x00000008 0x0000000c	Chip addr 0x0 0x000000004 0x00000008 0x000000000
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x0 0x00000004 0x00000008 0x0000000c 0x0000000c	Chip addr 0x0 0x000000044 0x000000006 0x00000000c 0x00000000c
Section vector.0 (48) vector.1 (47) vector.2 (46) vector.3 (45) vector.4 (44) vector.5 (43)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x0 0x00000004 0x00000008 0x00000000 0x00000010 0x00000014	Chip addr 0x0 0x00000004 0x00000008 0x00000000 0x00000000 0x00000010
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44) .vector.5 (43) .vector.6 (42)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x00000004 0x00000004 0x00000000 0x00000000	Chip addr 0x00000004 0x00000004 0x00000000 0x00000000
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44) .vector.5 (43) .vector.6 (42) .vector.7 (41)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x00000004 0x00000006 0x00000006 0x00000010 0x00000114 0x00000118 0x00000118 0x00000012	Chip addr 0x0 0x00000004 0x00000006 0x00000006 0x0000010 0x0000014 0x0000018 0x00000018 0x00000018
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44) .vector.5 (43) .vector.6 (42) .vector.7 (41) .mesbss.cinfo.n (4) 	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004	Space addr 0x0 0x00000004 0x00000000 0x00000000 0x00000000 0x00000000 0x00000010 0x000000110 0x000000110 0x000000110 0x000000110 0x000000110 0x000000110	Chip addr 0x0 0x000000004 0x00000000 0x00000000 0x00000010 0x00000018 0x00000012 0x00000012 0x00000012 0x00000020
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44) .vector.5 (43) .vector.5 (42) .vector.7 (41) .mestext.cinfo.getrevision (2) mestext.cinfo.getrevision (2)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x000000020	Space addr 0x0 0x0000004 0x0000008 0x0000008 0x0000001 0x0000011 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012	Chip addr 0x0 0x00000004 0x00000008 0x00000000 0x00000001 0x00000010 0x00000011 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012
<pre>Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.4 (44) .vector.6 (42) .vector.6 (42) .vector.7 (41) .mcsbss.cinfo.n (4) .mcstext.cinfo.getversion (1) .mcstext.cinfo.getversion (1)</pre>	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000000 0x000000020 0x00000020 0x00000020	Space addr 0x0 0x0000004 0x0000000 0x0000000 0x0000000 0x0000000 0x00000018 0x00000018 0x00000018 0x00000018 0x00000018 0x00000018 0x00000014 0x00000024 0x00000024 0x00000044	Chip addr 0x0 0x0000004 0x00000005 0x00000005 0x0000001 0x00000011 0x00000013 0x00000014 0x00000015 0x00000016 0x00000017 0x00000018 0x00000020 0x00000024 0x000000044 0x000000044
Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.5 (43) .vector.6 (42) .vector.7 (41) .mestext.cinfo.getversion (2) .mestext.cinfo.getversion (1) .mestext.libc.Evit (18)	Size (MAU) 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x00000004 0x000000004 0x000000020 0x000000020 0x000000020 0x000000020	Space addr 0x0 0x0000000 0x00000000 0x00000000	Chip addr 0x0 0x00000005 0x00000005 0x00000001 0x00000011 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000001 0x00000000 0x00000000 0x00000000 0x00000000
<pre>Section .vector.0 (48) .vector.1 (47) .vector.2 (46) .vector.3 (45) .vector.5 (43) .vector.6 (42) .vector.7 (41) .mestest.cinfo.getrevision (2) .mestext.cinfo.getrevision (1) .mestext.cinfo.main (3) .mestext.libcExit (18) .mestext.libcTART (17)</pre>	Size (MAU)	Space addr 0x0 0x0000004 0x00000004 0x00000000 0x00000000 0x00000001 0x00000010 0x00000001 0x00000001 0x00000001 0x00000010 0x00000010 0x00000010 0x00000010 0x00000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014 0x000000014	Chip addr 0x0 0x000000804 0x000000804 0x00000001 0x00000011 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000012 0x00000014 0x00000014 0x00000014 0x00000004 0x00000004 0x00000004

-8	Dissecombly 2 - Outline
cinfo_gtm30_05_mcs00.c 🛛	
⊕ * Generated by TASKING VX-toolset for MC ▲	Address: 0x000000
#include "cinfo gtm30 05 mcs00.h"	000000 78 00 00 e0 jmpSTART (0x78)
	000004 44 00 00 e0 jmp mcstext cinfo getversion (0x44)
unsigned long cinfo gtm30 05 mcs00[] = {	000008 24 00 00 e0 jmp mcstext cinfo getrevision (0x24)
0xE0000078, /* 0 */	00000c 0c 00 00 e0 jmp 0xc
0xE0000044, /* 1 */	000010 10 00 00 e0 jmp 0x10
0xE0000024, /* 2 */	000014 14 00 00 e0 jmp 0x14
0xE000000C, /* 3 */	000018 18 00 00 e0 jmp 0x18
0xE0000010, /* 4 */	00001c 1c 00 00 e0 jmp 0x1c
0xE0000014, /* 5 */ ≡	.sdecl '.mcsbss.cinfo.n'
0xE0000018, /* 6 */	000020 02 00 00 00 <illegal 00000002="" opcode=""></illegal>
0xE000001C, /* 7 */	movl r5,#2
0x00000000, /* 8 */	000024 02 00 00 15 mov] r5.0x00000002
0x15000002, /* 9 */	mur r5.0
0xA5020020, /* 10 */	000028 20 00 02 a5 mwr r5 0x00000020
0xA5800000, /* 11 */	mov r5.sta
0x55000002, /* 12 */	00002c 00 00 80 35 mov r5 sta
0xA8500000, /* 13 */	onl n5 #2
0xA2800000, /* 14 */	000020 02 00 00 55 001 05 000000002
0x42FFFFFE, /* 15 */	
0xA0200000, / 10 /	
0x15000005, / 1/ /	
0xA5820020, / 10 */	110V 12,5Ld
0x55000002 /* 20 */	000058 00 00 80 a2 mov r2,sta
0xA8500000 /* 21 */	
0xA2800000, /* 22 */	00005C TE TT TT 42 and1 r2,0X00TTTTTE
0x42FFFFFE, /* 23 */	mov stajr2
0xA8200000, /* 24 */	000040 00 00 20 as mov sta,r2
0x12000000, /* 25 */	movi r5,#3001
0xE0040000, /* 26 */	000044 by 0b 00 15 mov1 r5,0x00000bb9
0xA2800000, /* 27 */	mwr r5,n
10 01	000018 20 00 02 a5 mur r5 0x00000020

Figure 4 - Cross-referencing functions in a C array program

The symbol value for getrevision equals decimal 9. For an architecture with sizeof(long) equal to 4 this makes for an offset of decimal 36 or hexadecimal 24. Note that for this address the C array contains an instruction code of 0x15000002 which the simulator disassembly window translates to mov1 r5, 0x2 which is a preload of predefined MCS compiler macro __REVISION__ (since we used MCS v3.1r2) into register r5. Note that function getversion was coded with __channel(2), which means MCS address 0x000008 must contain a matching jump vector. This is achieved by MCS instruction code 0xE0000024 residing at decimal offset 9 within the C array.

ESTABLISHING THIRD-PARTY SYMBIOSES

the MCS program was downloaded properly and behaves as intended.

Once you have the C array footprint, copy it to your third-party compiler project and make sure it is located at its designated MCS base address. Each third-party declares this their own way but generally you'll find language extensions similar to the TASKING __at() keyword. You need to add this to the C array declaration yourself. Alternatively, you can leave the C array unscathed and use a locator equivalent. That's all it takes! The startup code of your toolchain will initialize the C array in the normal fashion, effectively bootstrapping the MCS program image into memory. Once that is all done, it only needs a little push to kick it into motion. You'll see this in the second part of the sample code in *Figure 5*.

As proof of concept we used the **TASKING VX-toolset for TriCore v6.0r1** to act as a third-party compiler and proceeded to incorporate the C array footprint. The snapshot on the next page shows what that looks like. Note the usage of _Pragma ("section fardata mcs00") to assure a unique section for the MCS C array. Also note that the linker script language (LSL) is subsequently used to anchor it to core mcs00. Finally, note what happens if you run it on an Infineon® TriBoard [2] using TASKING file system simulation (FSS). This will provide obvious proof that

cinfo_gtm30_05_mcs00.c 🛛	FSS 🕱
<pre>* "Generated by TASKING VX-toolset ^ #include "cinfo_gtm30_05_mcs00.h" _Pragma("section fardata mcs00"); unsigned long cinfo_gtm30_05_mcs00 %tE0000041, /* 0 */ %tE0000024, /* 2 */ %tE0000014, /* 4 */ %tE0000014, /* 5 */ %tE0000014, /* 6 */ %tE0000014, /* 6 */ %tE0000014, /* 6 */ %tE0000014, /* 8 */ %tE0000014, /* 8 */ %tE0000014, /* 8 */ %tE00000014, /* 8 */ %tE000000014, /* 8 */ %tE00000014, /* 8 */ %tE0000014, /* 8 */ %tE00000014, /* 8 */ %tE00000014, /* 8 */ %tE00000014, /* 8 */ %tE00000014, /* 8 */ %tE0000014, /* 8 */ %tE0000014, /* 8 */ %tE0000014, /* 8 */ %tE00000014, /* 8 */ %tE000000000000000000000000000000000000</pre>	C-array generated by: TASKING VX-toolset for MCS v3.1r2
avisaraaraa /* 1a */	4
<pre>// IASKING VA-COLISET TOT IFILORE // Eclipse project linker script file // Eclipse froject linker script file // Eclipse froject linker script file // Eclipse froject linker // Eclipse froject li</pre>	
<pre>section_layout mpe:tc0:linear { group mcs00_base (ordered,run_addr { select ".data.mcs00"; } }</pre>	r=addressof(mem:mpe:mcs00))
1	

Figure 5 - Code snapshot incorporating a C array footprint

It should be noted that because we used a TASKING compiler for testing, the SFRs used in the sample code are specific to TriCore[®] and will most likely be different from your primary architecture. There's also a chance that your third-party toolchain uses different keywords for the TASKING __interrupt and _Bool qualifiers. Some extra tweaks may be required before you can actually build and run the code.

The TASKING startup code for TriCore[®] automatically enables the MCS memory, whereas your third-party toolchain might leave that up to you. Whereas the TASKING toolset can immediately 'bootstrap' the code into MCS memory (provided the C array program image has been located properly at its base address) your third-party project will need user code to do that same copy.

If your third-party toolchain/debugger does not support a similar mechanism to TASKING file system simulation then you may not receive output from your debugger. If this happens you can restrict debugging to placing watches on variables version and revision.



CONCLUSION

The **TASKING VX-toolset for MCS** is the ideal partner when your third-party toolset is limited to code generation for the CPU of the hosting architecture. With its traditional linker C array output, the MCS toolset generates a pure ANSI-C application footprint that can be woven into the project of your primary CPU with little effort, other than making sure that it's located properly to its designated MCS base address. With the help of the TASKING standalone compiler for the GTM, you'll be able to enhance your development environment for programming complete RH850, Power Architecture or AURIX[™] based applications, regardless the C compiler used for the primary CPU.

Additional Resources:

[1] Bosch GTM IP Module. Web.

http://www.bosch-semiconductors.de/en/automotive_electronics/ip_modules/timer_ip_module/timer_platform_1.html

[2] Infineon TriBoard Development Boards.

http://www.infineon.com/cms/en/product/microcontroller/development-tools-software-and-kits/tricore-tm-development-tools-software-and-kits/aurix-starter-and-application-kits/channel.html?channel=5546d4614babddc8014bbc8126de00ad